REMARKS

Claims 39-41, 44-56, and 88-89 and 93-116 are pending in the application. Of these, claims 56, 88-89 and 112-116 were identified as allowed; claims 44-46, 54, 95-97, and 108 were identified as allowable if rewritten in independent form; and claims 39-41, 47-53, 55, 93-94, 98-107, and 109-111 stand rejected under 35 U.S.C. §102.

This amendment amends claims 51-53, 105-107, and 113. Claims 51-53 and 105-107 were amended to clarify correspondence of their preambles. Claim 113 was amended to ensure proper antecedence basis throughout the claim. (No subject matter was intended to be disclaimed or surrendered by these amendments.) Applicant requests respectfully that these amendments be entered because they not only put the claims in better form for appeal, but also do not raise any new issues requiring further search or substantive consideration.

Applicant reserves all applicable rights not asserted in or with this response, including, for example, the right to rebut tacit and explicit characterizations of one or more cited references, the right to rebut asserted combinations and motives for combinations, and the right to swear behind one or more cited references. Applicant makes no admissions regarding the status of any art of record as prior art.

Information Disclosure Statement

Applicant respectfully renews its request that the Examiner acknowledge consideration of the references submitted with the Information Disclosure Statement filed October 10, 2000 by returning an initialed copy of the corresponding 1449 Form with the next official communication.

Response to §102 Rejections

The Action rejects claims 39-41, 47-53, 55, 93-94, 98-107, and 109-111 under 35 USC § 102(e) as anticipated by Takenaka (U.S. 5,293,510). Specifically, the Action cites Takenaka features 32, 31, and 30 as corresponding respectively to the first, second, and third portions in the rejected claims.

In response, applicant submits respectfully that one of skill would not regard features 32, 31, and 30 as meeting the terms of the rejected claims, since each of the rejected claims requires "an electrode" comprising the first, second, and third portions, and Takenaka features 30-32 actually represent portions of two different electrodes.

More precisely, Takenaka Fig. 1 shows that features 31 and 32 adjoin each other to arguably represent a lower electrode (31/32) and that feature 30 represents an upper electrode. The upper and lower electrodes sandwich ferroelectric film 29 to define capacitor C. Neither the upper nor the lower electrode taken by itself includes first, second, and third portions. Thus, it does not appear that one of skill would read Takenaka Fig. 1 as teaching "an electrode" that meets the requirements of the rejected claims.

Accordingly, applicant requests respectfully that the Examiner reconsider and withdraw the §102 rejections of claims 39-41, 47-53, 55, 93-94, 98-107, and 109-111.

Conclusion

In view of the highlighted remarks, applicant respectfully requests reconsideration of the application. Moreover, applicant invites the Examiner to telephone its patent counsel (612-349-9593) to resolve any new issues that may delay allowance

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date 6 Jan 2003 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 6 day of January, 2003.

Tina Kraut
Name

_____
Signature

Docket No. 303.434US2
WD # 407329

Micron Ref. No. 92-0501.03

Clean Version of Pending Claims

METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS
Applicant: Pierre C. Fazan et al.
Serial No.: 09/489,954

Claims 39-41, 44-56, and 88-89 and 93-116, as of January 6, 2003 (date of Response to Final Office Action filed).

39. An electrode comprising:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above the upper surface; and

c) a third portion overlying said second portion and, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion are different materials.

40. The electrode as specified in Claim 39, wherein said second portion and said third portion are different materials.

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41. The electrode as specified in Claim 40, wherein the said first portion and the said third portion are different materials.

44. The electrode as specified in Claim 39, wherein said first portion is a silicon contact.

45. The electrode as specified in Claim 39, wherein said second portion is a diffusion barrier layer prohibiting diffusion of atoms between said first and said third portions.

46. The electrode as specified in Claim 39, wherein said third portion is an oxidation resistant layer.

47. The electrode as specified in Claim 39, wherein said insulative layer surrounds a lower sidewall of said third portion.

48. A dynamic random access memory device comprising:

an electrode which comprises:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above said upper surface; and

c) a third portion overlying said second portion and, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion are different materials.

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49. The electrode as specified in Claim 48, wherein said second portion and said third portion are different materials.

50. The electrode as specified in Claim 49, wherein said first portion and said third portion are different materials.

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51. (Amended) A dynamic random access memory device comprising:

a capacitor including an electrode which comprises:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above said upper surface; and

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c) a third portion overlying said second portion and, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion are different materials.

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52. (Amended) The dynamic random access memory device as specified in Claim 51, wherein said second portion and said third portion are different materials.

53. (Amended) The dynamic random access memory device as specified in Claim 52, wherein said first portion and said third portion are different materials.

54. The dynamic random access memory device as specified in Claim 51, further comprising:

a) a dielectric layer overlying said third portion; and

b) a cell plate electrode overlying said dielectric layer.

55. The dynamic random access memory device as specified in Claim 51 further comprising a transistor.

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56. An electrode comprising:

a) a contact formed in an insulative layer having an upper surface;

b) a diffusion barrier portion overlying said contact, said insulative layer surrounding a sidewall of said diffusion barrier portion and said diffusion barrier portion not extending above said upper surface ; and

c) an oxidation resistant portion overlying said diffusion barrier portion and, extending above and below said upper surface of said insulative layer, and including a recess, said diffusion barrier portion configured to inhibit diffusion of atoms between said contact and said oxidation resistant portion.

88. An electrode comprising:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above the upper surface; and

c) a third portion overlying said second portion, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion respectively consist essentially of polysilicon and tantalum.

89. The electrode as specified in Claim 88, wherein said third portion consist essentially of platinum.

93. An electrode comprising:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion and having a sidewall substantially flush with the upper surface; and

c) a third portion overlying the second portion, extending above and below the upper surface of the insulative layer, and including a recess, wherein the first portion and the second portion are different materials.

94. The electrode of Claim 93, wherein the second portion and the third portion are different materials.

95. The electrode of Claim 93, wherein the first portion is a silicon contact.

96. The electrode of Claim 93, wherein the second portion is a diffusion barrier layer.

97. The electrode of Claim 93, wherein the third portion is an oxidation resistant layer.

98. The electrode of Claim 93, wherein the insulative layer surrounds a sidewall of the third portion.

99. The electrode of Claim 93, wherein the insulative layer surrounds the sidewall of the second portion.

100. A dynamic random access memory device comprising:

an electrode which comprises:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion and having a sidewall substantially flush with the upper surface; and

c) a third portion overlying the second portion and, extending above and below the upper surface of the insulative layer, and including a recess, wherein the first portion and the second portion are different materials.

101. The electrode of Claim 100, wherein the second portion and the third portion are different materials.

102. The electrode of Claim 100, wherein the first portion and the third portion are different materials.

103. The electrode of Claim 100, wherein the first portion contacts the second portion, and the second portion contacts the third portion.

104. The electrode of Claim 100, wherein the insulative layer surrounds the sidewall of the second portion.

105. (Amended) A dynamic random access memory device comprising:

a capacitor including an electrode which comprises:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion and having a sidewall substantially flush with the upper surface; and

c) a third portion overlying the second portion and, extending above and below the upper surface of the insulative layer, and including a recess, wherein the first portion and the second portion are different materials.

106. (Amended) The dynamic random access memory device as specified in Claim 105, wherein the second portion and the third portion are different materials.

107. (Amended) The dynamic random access memory device as specified in Claim 105, wherein the first portion and the third portion are different materials.

108. The dynamic random access memory device as specified in Claim 105, further comprising:

a) a dielectric layer overlying the third portion; and

b) a cell plate electrode overlying the dielectric layer.

109. The dynamic random access memory device as specified in Claim 105 further comprising a transistor.

110. The electrode of Claim 105, wherein the first portion contacts the second portion, and the second portion contacts the third portion.

111. The electrode of Claim 105, wherein the insulative layer surrounds the sidewall of the second portion.

112. An electrode comprising:

a) a contact formed in an insulative layer having an upper surface;

b) a diffusion barrier portion overlying the contact and having a sidewall substantially flush with the upper surface; and

c) an oxidation resistant portion overlying the diffusion barrier portion and, extending above and below the upper surface, and including a recess, the diffusion barrier portion configured to inhibit diffusion of atoms between the contact and the oxidation resistant portion.

113. (Amended) The electrode of Claim 112, wherein the contact contacts the diffusion barrier portion, and the diffusion barrier portion contacts the oxidation resistant portion.

114. An electrode comprising:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion and having a sidewall substantially flush with the upper surface;

c) a third portion overlying the second portion, extending above and below the upper surface, and including a recess, wherein the first portion and the second portion respectively consist essentially of polysilicon and tantalum.

115. The electrode as specified in Claim 114, wherein the third portion consist essentially of platinum.

116. The electrode of Claim 114, wherein the first portion contacts the second portion, and the second portion contacts the third portion.